

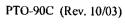


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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO	
10/005,471	11/06/2001	Syuji Otsuka	MES1P058	7233	
22434 759	90 08/06/2004		EXAM	EXAMINER	
BEYER WEAVER & THOMAS LLP			ELAMIN, ABD	ELAMIN, ABDELMONIEM I	
P.O. BOX 778			ART UNIT	PAPER NUMBER	
BERKELEY, C	CA 94/04-0//8	•	<u> </u>	PAPER NOMBER	
			2116 DATE MAIL ED: 08/06/2000		

Please find below and/or attached an Office communication concerning this application or proceeding.





•	•	Application No.	Applicant(s)	\$ /			
		10/005,471	OTSUKA, SYUJI	de			
	Office Action Summary	Examiner	Art Unit				
		A Elamin	2116				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply							
THE - External formula for a fer of the control of	ORTENED STATUTORY PERIOD FOR R MAILING DATE OF THIS COMMUNICATION Insigns of time may be available under the provisions of 37 Cl SIX (6) MONTHS from the mailing date of this communication of period for reply specified above is less than thirty (30) days, of period for reply is specified above, the maximum statutory properties to reply within the set or extended period for reply will, by the reply received by the Office later than three months after the end patent term adjustment. See 37 CFR 1.704(b).	ON. FR 1.136(a). In no event, however, may a on. a reply within the statutory minimum of this period will apply and will expire SIX (6) MON statute, cause the application to become A	reply be timely filed ty (30) days will be considered timely. NTHS from the mailing date of this com BANDONED (35 U.S.C. § 133).	munication.			
Status							
1)⊠	Responsive to communication(s) filed on	06 November 2001.					
2a) <u></u> □	This action is FINAL . 2b)⊠	This action is non-final.					
3)	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.						
Dispositi	on of Claims						
5) <u></u> 6)⊠	4) Claim(s) <u>1-9</u> is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration.						
	Claim(s) are subject to restriction a	ind/or election requirement.					
	on Papers						
9) The specification is objected to by the Examiner. 10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner.							
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
	Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).						
11)	The oath or declaration is objected to by th	•	• •	` '			
Priority u	ınder 35 U.S.C. § 119						
12)⊠ a)[Acknowledgment is made of a claim for for All b) Some * c) None of: 1. Certified copies of the priority docur 2. Certified copies of the priority docur 3. Copies of the certified copies of the application from the International Business of the attached detailed Office action for a	ments have been received. ments have been received in A priority documents have been ureau (PCT Rule 17.2(a)).	application No received in this National S	tage			
Attachmen	t(s)						
2) Notic 3) Infor	e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PTO-948 mation Disclosure Statement(s) (PTO-1449 or PTO/S r No(s)/Mail Date	Paper No(s	Summary (PTO-413) s)/Mail Date nformal Patent Application (PTO-1 	52)			

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DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

- (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
- 2. Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Takai, US. Pat. No. 6,373,307.
- 3. Claims 1, 3-4, 6 and 8-9, Takai teaches a pulse signal generating circuit for generating a specific pulse signal from a clock signal having a fixed cycle [abstract, Figs 1 and 2], comprising:

an edge detector [edge detector 11 of Fig. 1] configured to detect rising and trailing edges of the clock signal [CLK signal 1 of Fig. 1];

a first delay signal generator, including at least one first delay circuit having a first delay value, the first delay signal generator being configured to generate at least one first delay signal whose first delayed edge is delayed by the first delay value in relation to the rising edge of the clock signal [first delay circuit 112 of Fig. 1, abstract, col. 27, lines 11-13];

a second delay signal generator including at least one second delay circuit having a second delay value, the second delay signal generator being configured to generate at



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least one second delay signal whose second delayed edge is delayed by the second delay value in relation to the trailing edge of the clock signal [second delay circuit 212 of Fig. 1, abstract, col. 27, lines 21-24]; and

a logic unit configured to generate a pulse signal by performing logic operations on the first and second delay signals [Fig. 1, abstract, col. 14, lines 55-65].

- 4. Claims 2 and 7, Takai teaches a cycle duration of the pulse signal is set equal to a cycle duration of the clock signal [col.27, lines 14-16].
- 5. Claim 5, Takai teaches the edge detector comprises:

a first D flip-flop [Flip-Flop 12a of Fig. 2, col. 14, line 65 thru col. 15, line 23] having a first clock input terminal, a first D input terminal, a first non-inverted output terminal, and a first inverted output terminal, the clock signal being supplied to the first clock input terminal, an inverted output from the first inverted output terminal being fed back to the first D input terminal [Fig. 2]; and

a second flip-flop [Flip-Flop 12b of Fig. 2, col. 14, line 65 thru col. 15, line 23] having a second clock input terminal, a second D input terminal, second non-inverted output terminal, and a second inverted output terminal, an inverted signal of the clock signal being supplied to the second clock input terminal, an output from the first non-inverted output terminal of the first D flip-flop being supplied to the second D input terminal [Fig. 2];

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wherein an output from the first output terminal of the first D flip-flop is supplied to the first delay circuit, and an output from the second output terminal of the second D flip-flop is supplied to the second delay circuit [Figs. 1-2].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A Elamin whose telephone number is (703)305-3804. The examiner can normally be reached on MON-FRI 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (703) 308-1159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A Elamin Primary Examiner Art Unit 2116

August 3, 2004

A. ELAMIN
DV EXAMINER

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